C. REMARKS

Status of the Claims

Claims 8 - 27 are currently present in the Application, and claims 8, 15, and 21 are independent claims. Claims 1 - 7 have been canceled in response to a final restriction requirement. No claims have been amended or added in this Response.

Claim Rejections - Alleged Obviousness Under 35 U.S.C. § 103

Claims 8 - 27 stand rejected under 35 U.S.C. § 103 as allegedly being obvious, and therefore unpatentable, over U.S. Patent No. 6,366,109 to Shigeru Matsushita (hereinafter "Matsushita") in view of U.S. Patent No. 4,292,668 issued ***September 29, 1981*** to Miller et al. (hereinafter "Miller"). Applicant respectfully traverses the rejections.

Prosecution History

The previous Office Action, dated December 30, 2005, cited the primary reference (Matsushita) in rejecting Applicants' claims under 35 U.S.C. § 102. On March 30, 2006, Applicants responded without modifying any claims and pointed out that Matsushita simply did not teach or suggest the limitations found in each of Applicants' independent claims. The present Office Action attempts to shore up the severe shortcomings of Matsushita by combining the teachings of Matsushita with those of Miller. Applicants note that Miller issued on ***September 29, 1981, over a quarter of a century ago.*** Nonetheless, in the paragraphs below Applicants explain why the combination of Matsushita in view of Miller also does not teach or suggest the limitations found in Applicants' independent claims.

MPEP § 2143.03, requires that the references cited in the Office Action teach "each and every" element of Applicants'

claimed invention. However, as explained in detail below, neither Matsushita nor Miller, taken alone or in combination with one another, teach each and every element included in Applicants' independent claims. Consequently, Applicants' claimed invention is allowable over Matsushita in view of Miller.

In Applicant's independent claims, Applicant claims a method, information handling system, and computer program product that each include limitations of:

- receiving a first assignment request;
- identifying one or more interface pins that correspond to the first assignment request;
- selecting a first interface controller from a plurality of interface controllers that correspond to the first assignment request; and
- associating the identified interface pins with the selected interface controller.

In contrast to the limitations claimed in each of Applicant's independent claims, Matsushita teaches a semiconductor device testing system that, among other shortcomings, simply does not teach "selecting … [an] interface controller…" nor does Matsushita teach or suggest Applicant's claimed limitation of "associating the identified interface pins with the selected interface controller."

The Office Action contends that Matsushita teaches these limitations. However, as discussed below, the Office Action's reliance on Matsushita is misplaced.

Matsushita teaches "a semiconductor testing device for testing a semiconductor with a plurality of pins by applying a test signal." Figure 4 of Matsushita shows a configuration of Matsushita's pin assignment converter:

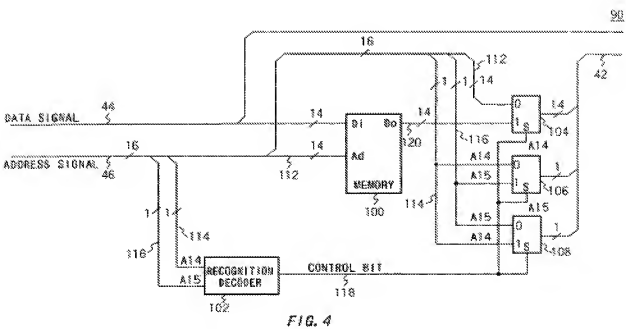

FIG. 4

The Office Action contends that Matsushita teaches Applicant's claimed limitation of "selecting a first interface controller from a plurality of interface controllers that correspond to the first assignment request," citing Matsushita's multiplexers (104, 106, and 108). While multiplexers are used for selecting data, the multiplexers used by Matsushita do not teach anything regarding selecting an "interface controller from a plurality of interface controllers," as claimed by Applicant. Instead, Matsushita uses the multiplexers to either replace an address signal (46) with output data (120), or leave the addresses unchanged (Matsushita, col. 6, lines 36-57). In this manner, Matsushita teaches that different semiconductor devices

can be tested by replacing the pin assignment data in the pin map memory (col. 6, line 58 – col. 7, line 4).

While Matsushita may teach a system for testing semiconductor chips that are packed in different types of packages using the same test vectors and test programs (col. 6, lines 57-60), Matsushita teaches nothing regarding selecting an "interface controller from a plurality of interface controllers," as taught and claimed by Applicant. It follows that, because Matsushita is void of any teaching regarding selecting interface controllers, Matsushita is also void of any teaching regarding associating identified interface pins with a selected interface controller.

In the present Office Action, the Examiner no longer contends that Matsushita's "recognition decoder" is analogous to Applicant's interface controller. Instead, the present Office Action asserts that Matsushita's recognition decoder "has the functionality to proceed with the means for associating," found in Applicants' independent claims. Applicants disagree. Applicants' full limitation reads "means for associating the identified interface pins with the ***selected interface controller***" (emphasis added). As Applicants previously explained, Matsushita does not teach or suggest multiple interface controllers, so it follows that Matsushita does not teach or suggest "associating" any pins with a "selected interface controller." Therefore, Matsushita's "recognition decoder" is not analogous or in anyway interchangeable with Applicant's claimed "interface controller" that is selected from a *plurality of interface controllers*.

The present Office Action now admits that Matsushita does not teach or suggest a system having a plurality of interface

controllers. The present Office Action also admits that Matsushita does not teach or suggest Applicants' claimed limitation of "selecting a first interface controller from the plurality of interface controllers that correspond to the first assignment request." Instead, the Office Action attempts to combine the teachings of Matsushita with those of Miller and reasons that just because Miller teaches a plurality of interface controllers, the combination of Matsushita and Miller render Applicants' claimed invention obvious. Applicants disagree.

In the cited section of Miller, Miller teaches an improvement to a "DMA IOC" (also known as a "DMA Controller"). Older systems, such as those described by the 25-year old Miller patent, often used DMA Controllers to communicate with I/O devices (such as printers, etc.). This was because I/O devices are very slow in comparison to the CPU, and older architectures would have the CPU spending large amounts of computer time sitting idle waiting for data from the I/O device. The DMA controller addressed this problem by providing a low-cost CPU that had enough logic and memory to handle such I/O tasks. Because these controllers had direct access to the memory, they are often referred to as "Direct Memory Access" (DMA) controllers. Modern computer systems are much faster and more complex than the computer system Miller described in his 1981 patent. Today's computers no longer "block" when waiting for data, unlike most computers that used DMA controllers.

Despite the fact that Miller is a relatively ancient piece of prior art discussing a type of controller that is not in widespread use today, nowhere does Miller teach or suggest "receiving an … assignment request," "identifying … interface

pins that correspond to the … assignment request," "selecting a … controller … that corresponds to the assignment request," nor does Miller teach or suggest "associating the identified pins with the selected interface controller."

> Main memory 1, 214-1, containing 48 K words and main memory 2, 216-1 containing 16 K words, are connected to system bus B 204. Memory save unit 222 is also connected to system bus B 204. System bus A 202 and system bus B 204 are connected to CPU 200, control panel 201 is directly connected to CPU 200. Diskette peripheral devices 1 and 2, 207-1 and 207-2, are connected to system bus A 202 via diskette controller 1, 206-1. Diskette peripheral devices 3 and 4, 221-1 and 221-2, are connected to system bus B 204 via diskette controller 220-1. Communication lines 1 and 2 are connected to system bus A 202 via communications controller 210-1. Printer peripheral device 209 is connected to system bus A via printer controller 208-1. The console peripheral device 213 is connected to system bus A 202 via console controller 212-1. It should be noted that a like numbered element in one figure refers to the same numbered element in another figure; for example, control panel 201 in FIG. 2 refers to the same element as shown as control panel 201 in FIG. 1.

Other than the system taught by Miller having more than one interface controller, it does not teach or suggest any of Applicants' other limitations set forth in each of Applicants' independent claims. The cited section reiterates the fact that Miller is a very old prior art reference that teaches a mainframe system with 48K of main memory.

The combination of Matsushita and Miller clearly fails to teach or suggest each limitation of Applicant's claimed invention. Instead, Matsushita teaches a system that tests semiconductor chips but does not teach anything regarding more than one interface controller or how to identify an interface controller based upon a pin assignment. Miller is a very old

patent and, other than having more than one interface controller, does not teach or suggest any of Applicants' claimed limitations. As described above, the combination of Matsushita in light of Miller fails to teach or suggest at least two of Applicant's claimed limitations found in each of Applicant's independent claims. Therefore, claims 8, 15, and 21 are each allowable over Matsushita in view of Miller.

Each of the remaining claims depends, directly or indirectly, on an allowable independent claim. Therefore, each of the dependent claims are also allowable for at least the same reasons as the independent claims are allowable.

Conclusion

As a result of the foregoing, it is asserted by Applicants that the remaining claims in the Application are in condition for allowance, and Applicants respectfully request an early allowance of such claims.

Applicants respectfully request that the Examiner contact the Applicants' attorney listed below if the Examiner believes that such a discussion would be helpful in resolving any remaining questions or issues related to this Application.

Respectfully submitted,

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